

Appl. No. 10/607,633
Amdt. dated April 4, 2005
Response to Office Action of January 4, 2005

PATENT

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claims 1.-6. (Canceled).

Claim 7. (Currently Amended) A method of making a chip device, the method comprising:
providing a leadframe that includes leads;
providing a die that includes a backside, wherein the backside of the die forms ~~an~~
a first electrical terminal;
coupling a frontside of the die to the leadframe with solder, wherein the frontside of the die comprises a second electrical terminal, wherein first electrical terminal and the second electrical terminal are terminals in a MOSFET device; and
encapsulating the die with a body such that the backside of the die is adjacent to a window defined within the body.

Claim 8. (Currently Amended) A method in accordance with claim 7 wherein after encapsulating, ends of the leads of the leadframe are substantially coplanar with the backside of the die ~~further comprising configuring the plurality of leads.~~

Claim 9. (Original) A method in accordance with claim 8 further comprising removing dambars from the leadframe, removing mold flashes and resins from the leads, and solder plating the leads.

Claim 10. (Original) A method in accordance with claim 7 further comprising marking the body on a surface opposite the window.

Claim 11. (Original) A method in accordance with claim 10 wherein the marking is performed with a laser.

Appl. No. 10/607,633
Amdt. dated April 4, 2005
Response to Office Action of January 4, 2005

PATENT

Claim 12. (Original) A method in accordance with claim 10 wherein the marking is performed with ink.

Claim 13. (Original) A method in accordance with claim 7 wherein the leadframe is provided with preplated leads.

Claim 14. (Original) A method in accordance with claim 7 wherein the leadframe is provided with preformed leads.

Claim 15. (Original) A method in accordance with claim 7 wherein the leadframe is provided with preplated leads and preformed leads.

Claim 16. (Previously Presented) A method in accordance with claim 7 wherein the die is coupled to the leadframe via solder bumps, and wherein the solder bumps are re-flowed.

Claim 17. (Previously Presented) A method in accordance with claim 7 wherein the die is a first die and wherein the method includes attaching a second die to the leadframe.

Claim 18. (Currently Amended) A method comprising:
providing a leadframe that includes leads;
providing a semiconductor die that includes a backside including a first electrical terminal and a frontside including a second electrical terminal, wherein the first electrical terminal and the second electrical terminal are terminals in an electrical device;
mounting the semiconductor die to the leadframe; and
encapsulating the semiconductor die and at least a portion of the leadframe with a molding compound having a window and an exterior surface, wherein the backside of the semiconductor die is exposed through the window of the molding compound and wherein the backside is substantially flush with the exterior surface of the molding compound.

Appl. No. 10/607,633
Amdt. dated April 4, 2005
Response to Office Action of January 4, 2005

PATENT

Claim 19. (Currently Amended) The method of claim 18 wherein the electrical device is semiconductor die comprises a power transistor.

Claim 20. (Previously Presented) The method of claim 18 further comprising:
mounting a second semiconductor die including a second backside to the leadframe, wherein second backside is exposed through a second window in the molding compound.

Claim 21. (Previously Presented) The method of claim 18 wherein mounting the semiconductor die to the leadframe includes using solder to mount the semiconductor die to the leadframe.

Claim 22. (Currently Amended) The method of claim 18 wherein the semiconductor die comprises second electrical terminal is a source and or gate terminal at the frontside terminals at a side opposite the backside.

Claim 23. (Previously Presented) The method of claim 18 wherein the leadframe is pre-plated.

Claim 24. (Previously Presented) The method of claim 18 wherein ends of the leads are co-planar with the backside of the semiconductor die.

Claim 25. (Previously Presented) The method of claim 18 wherein the backside of the semiconductor die is metallized.

Claim 26. (Currently Amended) The method of claim 26 18 wherein the device is a MOSFET, and wherein the backside forms a drain terminal of [[a]] the MOSFET in the die.